Aum HPC Processor

Development under National Supercomputing Mission

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Brief about National Supercomputing Mission

• **Supercomputing infrastructure** in the country

• **Indigenous Supercomputing ecosystem** in phased manner: From “Assembly” to “Manufacturing” to “Design and Manufacturing” of Supercomputers
  - Servers
  - HPC network
  - Software stack
  - HPC Processor
  - Liquid cooling technologies

• **Supercomputing Applications** of National interest

• **Human resources** for applications development and HPC maintenance
Motivation for India’s own HPC Processor - AUM

• Processor architecture suitable for both HPC & General Purpose Computing - Extracting maximum application level performance

• Energy efficiency: Arm Architecture

• Capability building with bargaining power

• Immunity from possible export restrictions to India in Future

• Technological sovereignty: Designed and Engineered in India

• Security (Back doors etc.) : Highest priority for strategic sectors
HPC Processor development program

• Develop a competitive HPC Processor for HPC, AI and server market
• Develop a complete ecosystem leveraging open source components
  • Open source software ecosystem
  • Reference Boards
  • Reference server designs
• Build a Pilot HPC system with > 1 PF compute power
• Be ready with Exascale system design and subsystems based on AUM Processor
• Industry Collaboration – Design of SoC, Server designs, Deploy and market solutions based on AUM Processor
• Targeted for both HPC and Cloud market
• Planned to be available in 2024
Some of the Architectural decisions

- **Best Efficiency**
  - Memory Bandwidth
  - Easy to optimize (Vector Size)
  - Superior Application level program / Watt

- **Better I/O for Data Access**
  - HBM and DDR
  - Many PCIe5 Lanes
  - CXL for Coherent accelerators

- **No Competition with specialized devices like GPUs** – Keep Provision of GPUs for specialized applications

- **Security Features Provision**

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- **Superior Application level program / Watt** -> Increase Memory sub-system performance

- **Need Much better Bytes/Flop performance** – Target > 0.5 Byte/Flop
# High Performance Conjugate Gradients (HPCG) Benchmark

<table>
<thead>
<tr>
<th>Rank</th>
<th>Site</th>
<th>Computer</th>
<th>HPL Rmax (Pflop/s)</th>
<th>Bytes/Flop</th>
<th>HPCG (Pflop/s)</th>
<th>Fraction of Peak</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RIKEN Center for Computational Science, Japan</td>
<td><strong>Supercomputer Fugaku</strong> — A64FX 48C 2.2GHz, Tofu D</td>
<td>442.01</td>
<td>0.3</td>
<td>16</td>
<td>3.00%</td>
</tr>
<tr>
<td>2</td>
<td>DOE/SC/ORNL, USA</td>
<td><strong>Summit</strong> — IBM POWER9 22C 3.07GHz, Dual-rail Mellanox EDR Infiniband, NVIDIA Volta GV100</td>
<td>148.6</td>
<td>&lt;0.2</td>
<td>2.926</td>
<td>1.50%</td>
</tr>
<tr>
<td>3</td>
<td>DOE/SC/LBNL/NERSC, United States</td>
<td><strong>Perlmutter</strong> — AMD EPYC 7763 64C 2.45GHz, Slingshot-10, NVIDIA A100 SXM4 40 GB</td>
<td>64.59</td>
<td>&lt;0.2</td>
<td>1.905</td>
<td>2.10%</td>
</tr>
<tr>
<td>4</td>
<td>DOE/NNSA/LLNL, USA</td>
<td><strong>Sierra</strong> — IBM POWER9 22C 3.1GHz, Dual-rail Mellanox EDR Infiniband, NVIDIA Volta GV100</td>
<td>94.64</td>
<td>&lt;0.2</td>
<td>1.796</td>
<td>1.40%</td>
</tr>
</tbody>
</table>

**K-Computer**: Bytes/Flop = 0.5  
HPCG – 5.2% of Peak

Superior Application level program  
Better Bytes/Flop i.e. higher Memory B/w
C-DAC HPC SoC (A48Z) Block Diagram (48-Cores)

- Arm Neoverse V1 (Zeus)
- Arm Zeus Cores (48)
- PCIe Gen5 / CXL
- D2D SubSystem (Fully Coherent)
- C2C SubSystem (Fully Coherent)
- CortexM7 based MSCP SubSystem
- Coherent Mesh Network
- System Cache
- Other Chiplet
- Other Socket
- (Memory Subsystem) HBM3, DDR5
- Security SubSystem
C-DAC AUM Microprocessor – 96 Cores

- **HBM3 5600 RAM**
- **A48Z** (Chiplet-1) 48-Zeus Cores, 8-DDR5 Channels
- **D2D Chiplet Interconnect**
- **Interposer**
- **HBM3 6400**
- **DDR5-520**
- **PCIe Gen5/CXL**

- **HBM3 6400**
- **A48Z** (Chiplet-2) 48-Zeus Cores, 8-DDR5 Channels
- **D2D Chiplet Interconnect**
- **Interposer**
- **HBM3 6400**
- **DDR5-520**
- **PCIe Gen5/CXL**
AUM - HPC Processor Development

• 96 core HPC Processor
  • ARM 8.4 architecture
  • 96MB L2 cache, 96MB System cache
  • 8 channel 5200 Mhz DDR5 memory
  • 64 GB HBM3 5600Mhz memory
  • PCIe5 64/128 Lanes – CXL support for coherent Accelerators/ NIC
  • SMP support up to 2 sockets
  • Security Features - Secure boot and Crypto support
  • 5nm Technology Node, Chiplet based architecture, 2-Chiplets, 96-Cores and up to 96-GB HBM3 memory in a socket

• Dual socket Server design with up to 4 Industry standard GPU accelerators – Both HPC and AI applications (CPU Only node ~ 10 TF/Node)

• Indigenous Software eco-system for Aum Processor leveraging open source eco-system
## Specification Comparison

<table>
<thead>
<tr>
<th></th>
<th>Fujitsu A64FX</th>
<th>C-DAC AUM HPC Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Fabrication Technology</strong></td>
<td>7nm FF TSMC</td>
<td>5nm FF</td>
</tr>
<tr>
<td><strong>Core Configuration</strong></td>
<td>(48+4)-Cores, 2.2 GHz (typical)</td>
<td>96-Cores, 3.0 GHz (typical) 3.5+ GHz (turbo)</td>
</tr>
<tr>
<td><strong>DDR Configuration</strong></td>
<td>No DDR</td>
<td>16-Channels (32 bit) DDR5-5200 BW = 332.8 GB/s</td>
</tr>
<tr>
<td><strong>HBM</strong></td>
<td>32-GB HBM2 (4-Controllers) BW = 1 TB/s</td>
<td>64-GB HBM3 (4-Controllers) BW = 2.87 TB/s</td>
</tr>
<tr>
<td><strong>PCIe</strong></td>
<td>16 PCIe Gen3 Lanes</td>
<td>64 PCIe Gen5 Lanes</td>
</tr>
<tr>
<td><strong>Power</strong></td>
<td>Not Known</td>
<td>300 W (TDP)</td>
</tr>
<tr>
<td><strong>Performance (DP)</strong></td>
<td>2.7 TFLOPS per socket</td>
<td>4.6+ TFLOPS per socket</td>
</tr>
<tr>
<td><strong>Bytes/FLOPS</strong></td>
<td>0.38</td>
<td>0.7</td>
</tr>
</tbody>
</table>
C-DAC HPC System SW & Development Tools

- System Software, Dev Tools and Utilities
  - HPC Compiler (C and Fortran, multicore + accelerator, HPC & AI applications)
  - IDE for HPC & AI applications on ARM system supporting multiple parallel paradigms
  - Automatic Parallelizer generate parallel code for multicore / accelerators
  - Application Debugger & Profiler
  - Optimized Math-AI Libraries
  - ARM System Monitor and Utilities
  - Parallel Runtime System
  - Secure Access Interface

- HPC System Middleware

- HPC Applications
Summary Aum Processor

- Competitive HPC Processor for HPC, AI and server market
- Address Strategic requirements
- Complete ecosystem
  - Open source software ecosystem
  - Reference Boards
  - Reference server designs – Derivatives as per market requirements
  - Industry partners OEMs/ODMs/Solution providers
- Towards Indigenous Exascale system including Processors
- Targeted market HPC/AI, Cloud, storage, edge computing
- Planned to be available in 2024
Thank You
<table>
<thead>
<tr>
<th></th>
<th>Ampere Altra</th>
<th>SiPearl Rhea</th>
<th>C-DAC ³⁵</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cores</strong></td>
<td>80 Arm Neoverse N1 (Ares) Cores</td>
<td>72 Arm Neoverse V1 (Zeus) Cores</td>
<td>96 Arm Neoverse V1 (Zeus) Cores</td>
</tr>
<tr>
<td><strong>Cache</strong></td>
<td>L1: 64 KB L1 I / 64 KB L1 D Cache per core</td>
<td>System Cache: 128 MB</td>
<td>L1: 64KB I-Cache / 64KB D-Cache per Core</td>
</tr>
<tr>
<td></td>
<td>L2: 1 MB L2 cache per core</td>
<td></td>
<td>L2: 1MB Unified Cache per Core</td>
</tr>
<tr>
<td><strong>Frequency</strong></td>
<td>3.0 (base), 3.3 GHz (turbo)</td>
<td>2.5 GHz (base), 3.0 GHz (turbo)</td>
<td>3.0 Ghz</td>
</tr>
<tr>
<td><strong>HBM</strong></td>
<td>No HBM</td>
<td>96GB of HBM2E</td>
<td>96GB of HBM3</td>
</tr>
<tr>
<td><strong>DDR</strong></td>
<td>up to 4 TB per socket.</td>
<td>4 Channels DDR5</td>
<td>16 Channles DDR5</td>
</tr>
<tr>
<td><strong>PCI</strong></td>
<td>128 PCIe4 Lanes</td>
<td>104 Lanes PCIe5:</td>
<td>128 Lanes PCIe5:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Upto 64-lanes for coherent connectivity</td>
<td>- Upto 64-lanes for coherent connectivity</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Remaining lanes as PCIe5</td>
<td>- Remaining lanes as PCIe5/CXL</td>
</tr>
<tr>
<td><strong>TDP</strong></td>
<td>250 W</td>
<td>320W</td>
<td>280 - 320 W</td>
</tr>
<tr>
<td><strong>Node</strong></td>
<td>TSMC 5nm</td>
<td>TSMC 6nm</td>
<td>TSMC 5nm</td>
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<td><strong>Package</strong></td>
<td>2.5 D</td>
<td>2.5D</td>
<td>2.5D</td>
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<tr>
<td><strong>Release Year</strong></td>
<td>2020</td>
<td>2022 /23</td>
<td>2023 / 24</td>
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