SHAKTI - An Indigenous RISCV Microprocessor from Bharat

V. Kamakoti,
Professor of Computer Science and Engineering, IIT Madras
Prathap Subrahmanyam Centre for Digital Intelligence and Secure Hardware Architecture
RISE Group
Indigenous Microprocessor Development Program
Early 2012:
Deliver something we can that will benefit our Country - Not just ABSTRACT but a Life-Line product by 2020
Processor was the obvious choice
Background

Instruction Set Architecture

Complex Hardware (CISC)

Simple Software

Complex Software

Simple Hardware (RISC)

CISC: Intel, AMD, IBM, SPARC

RISC: MIPS, ARM

CISC failed in mobile/IoT platform - power consumption issues

RISC succeeded in Mobile/IoT and entering the laptop/Desktop/server game - Software is a easy nut to crack.
• The birth of RISCV
  • Berkeley and MIT started the effort - RISCV consortium
  • From India, IITM was one of the very early founding members
The Initial Thoughts

• Should be Marketable - compete with the BILLION Dollar Processor Industry
• Manpower - can we do it with a small team?
• Software + Hardware - make a processor - should we do both?
Initial Decisions - 2012/13

• We need to go with open source software stack - that is verifiable
• We need to take up a hardware for which software is already stable and make the hardware
• The Machine Language - Instruction Set Architecture (ISA)
• Started with IBM Power - Open Power - thus the name “SHAKTI”
• Too much legacy - not fitting to 2020 Deadline
• Funding?? Billions of dollars for such processors
The SHAKTI Program

• Berkeley/MIT team reached us and we started the program -
  • Happy to note that in the year 2020 - Prof Patterson (Berkeley - ACM Turing award winner 2020) in his “One decade History of RISCV” talk has taken up SHAKTI as a key development.
  • Link to the video

• Advantages

Open Source ISA, No encumberance, No sanctions
Software developed globally
Crucial Decision:
  India’s microprocessor should be RISCV?
  How will it be in 2020?
The strength of the RISCV gave us the confidence
We proposed in 2015 to Melty, Gol that we must go with RISCV
My First Dedicated IITM Team

They have given up and continue to give up BIG SALARIES in MNCs and to realize the SHAKTI Vision
SHAKTI - Roadmap

Distributed AI/ML - Inspired

D1: Environment monitoring
D2: Industry 4.0 Process control, Vehicular Electronics, POS
D3: Network Routers, Mobile Phones, Desktops, Workstations
D4: Cloud, Transaction Processing, Supercomputing
## The SHAKTI Family

### ‘E’ Class
- **32/64-bit Embedded 3-stage Pipeline**
  - (Sub 200 MHz - IOT End Devices)
  - QSPI, UART, I2C, PWM – RTOS
- Status: Developed, FPGA (4K LUTs), Ready for ASIC Tapeout
- Market Equivalence: ARM Cortex M-series

### ‘C’ Class
- **32/64-bit 5-stage Pipeline (Industrial Controllers, PoS, Storage Controllers)**
  - I2C, UART, DMA, MMU, QSPI, SDRAM Linux Booted, SEL4 boot in progress
- Status:
  - FPGA (18K LUTs) + RISECREEK ASIC (22nm FinFET) Intel; RIMO ASIC (180nm) SCL,
  - RISECREEK Details: Size: 16 mm², DMIPS/MHz – 1.67
  - 16KB L1 split I- and D- caches
  - Vcc - 0.75V, Clock: 350 MHz
- Market Equivalence: ARM A35, A55, Intel Atom

### ‘I’ Class
- **64 Bit RISC-V Based 12 Stage Pipelined, Dual Issue, Out-of-Order execution**
- Status: Developed under verification, FPGA Prototype: Jan 2019
  - ASIC Tapeout readiness: Mar 2020
- Market Equivalence: ARM A9, A15

### ‘T’ Class (Security)
- **64 Bit RISC-V 5-stage pipeline, secure Variant, Changes to LLVM**
- Status: Developed under verification, FPGA Prototype: Dec 2021
  - ASIC Tapeout readiness: Mar 2021
- Market Equivalence: Novel

### ‘F’ Class (Fine grain Fault Tolerance)
- Status: Prototype Design
- Published
- Market Equivalence: Novel

### ‘S’ Class (AI/ML compatible)
- **AI Accelerators**
- Status: Developed, under verification
- Market Equivalence: Novel
Deep embedded, extreme low power with optional low power radio, NAVIC.

Edge and deep embedded devices.

Specialized ultra low power variants can be designed to use power harvesting.

Standard embedded SoCs with 1-8 in-order cores

Capable of running RTOSs and MMU based OSs like Linux or Secure L4.

Mobile/Desktop grade SoCs with 1-8 in-order/OO cores,

VPUs and optional AI/ML accelerators and GPUs.

Secure mobile, desktops and high power embedded applications, low end servers

Secure Server SoCs with 2-32 OO cores,

VPUs and optional AI/ML accelerators.
The MDP Project - IITM

• IITM Approached MEITY for funding for developing the E/C/I classes of cores
• Funding of 7 crores sanctioned in Nov 2017 to IITM + 4 crores to SCL, Chandigarh by MEITY
The Shakti Moments
In the year 2018

- SoC Config:
  - 2x (UART, I2C, QSPI).
  - SDRAM Controller, DMA, TCM (128Kb)
  - JTAG Based Debugger.
- Operating Voltage: 0.7V
- Operating Frequency: 300MHz
- I/O Dominated Design: 320 IOs
- Area: ~100K Gates for Core +200K for SoC

C-Class Tapeout @ Intel Oregon 22FFL

RISE CREEK
In the year 2018

RIMO:

- 4KiB Cache instead of 16KiB
- 256KiB on-chip SRAM instead of 128KiB
- No SDRAM

C Class Tape out Fabricated at SCL, Chandigarh 180nm
In the year 2020

Aardonyx:
- Die size 5387*5227um
- Gate Count 646K
- Clock frequency is 100MHz
- CQFP 256 pin package

E Class Tape out Fabricated at SCL, Chandigarh 180nm Four Metal Process Technology

Features of Moushik E Class
- PWM x 6
- SPI x 3 (ADC/SDCARD/A_H)
- GPIO x 16
- UART x 3
- QSPI x 1 (FLASH)
- I²C x 2 (EEPROM/A_H)
- SDRAM 32-bit
- JTAG x 1
- FREQUENCY: 100Mhz

Bootup video Link
SHAKTI-SafeRV Quad core Boot on FPGA - THALES
The Key Enablers

The Special Manpower Development Program (SMDP VLSI of MEITY)

- CAD tool availability
- Manpower training and availability
- Thousands of Students benefitted - both Research and Course-work
- Several basic and advanced courses run on the tools provided by this program

- Description of the design
- It is open source
- 250X more productivity
- FORMAL VERIFICATION POSSIBILITY
- RULE Based designs - fixes issues at early stage
- Bluespec Compiler ensures no race condition designs, deadlock free, intent-faithful designs.
Key Deliverables

- Three chips
- IGCAR - removal of Motorola without major change in other hardware components (The VME interface) and NIL changes in software. Successful field trials (One year Zero errors)
- ISRO - IISU chip + NAVIC
- Thales - Fault-tolerance effort
- Swadeshi Microprocessor Challenge
- Adoption by ALTAIR, USA
Software Development Activities

Software Development Kit
- Support for current versions of C and E class.
- **Driver support** for PLIC, CLIC, SPI, QSPI, UART, I2C and PWM.
- Standalone mode supported on E class.
- Multilevel logging, Direct Flash programming, MMU support added.
- ESP8266 & ESP 32, FTDI, External Flashes and many sensors integrated.
- IoT support added and live temperature monitoring done using SHAKTI.
- Arduino compatible board and peripheral support added.

Highlights of the SDK
- Clean separation between drivers, boot, core and application layers
- Easily portable to **any RISC-V based architecture**
- **Multiple sensors** connected and proven with SHAKTI-SDK.

OS Support
Using Arty-7100T with SHAKTI

STEP 1: Prerequisites

Note: Please ensure SHAKTI C Class is programmed onto the Arty-7 100t board.

1. Install the required packages.
   
   ```
   sudo apt-get install python-serial
   ```
   
   If you face any error while running any command, please refer FAQ section.

2. Please ensure SHAKTI toolchain is installed successfully.
   
   ```
   which riscv64-unknown-elf-gcc
   ```
   
   ```
   /path-to-shakti-tools/bin/riscv64-unknown-elf-gcc
   ```
   
   ```
   which opendoa
   ```
   
   ```
   /path-to-shakti-tools/bin/opendoa
   ```

3. Please connect Arty-7 100t board to the system using the microUSB cable.
Additional Efforts and Interest

- Edge AI and security taken up by IITM as the next project funded by Melty with a value of 9 crores.
- DRDO interested in D1, D2, D3 and D4
- ISRO has sanctioned a project to map AI algorithms onto SHAKTI based edge AI Accelerator
- SAMSUNG has shown interest in taking up SHAKTI for their consumable electronics - two meetings completed and positive.
- Talks in progress for developing the SPRESENSE board of Sony using SHAKTI (Currently with ARM)
Configurable Hardware Enforced Security and Separation (CHESS)

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- Lynx Works: Only one major vendor for SK in the world so far.
- CHESS is from SecureWeave, a Bangalore based startup and successfully demonstrated SK on x86 platform.
- Porting is currently done on SHAKTI platform.
- Exploits the Hypervisor mode of SHAKTI and will be integrated with High Assurance Boot framework.
RISC-V (RISC-Five) is not RISC => The RISCy Evolution

RISC 1 (1981) From Berkeley

- Simple ISA
- Clean-slate ISA
- Modular ISA
- Extensible ISA
- Stable ISA

3GPP of Computing

IIT Madras - Contribution to RISC-V Foundation

RISC-V and IIT Madras
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