VEGA Processors

Making India AtmaNirbhar in Swadeshi Compute Designs

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C-DAC
CDAC – R&D organisation under MeitY
Hardware Design Group – Thrust Areas

- Product designs for Industrial, Consumer, Automotive and Bio-Medical Applications
- Total product implementations using ASIC Technology
- IP development for ASIC implementations
- ASIC Consultancy Services
- Design Verification Services
Expertise

- Microprocessor Design
- ASIC design and FPGA implementations
- Analog and Mixed Signal IC design
- High speed PCB design
- Embedded System development
- Ergonomics, tooling and mechanical design
- Precision assembly and testing
- Field deployment of products and ToT
ASTRA – IP Portfolio

- EROTG1: USB On-The-Go
- ERUSB2: USB Host / Device Controller
- ERSDRAM: SDRAM Controller
- ERPCIe: PCI Express Endpoint
- ERSATAII: SATA Host Controller
- ERMAC: 10 / 100 /1000
- ERSDHC: SDHost Controller
- ER15530: Manchester Encoder Decoder
- ER-eMMC: eMMC Controller
- ER146818: Real Time Clock
- ERTIMER: Timer
- ER16C450: UART
- ERSPI: SPI
- ERQSPI: QSPI
- ERPWM: PWM
- ERI2C: I2C
- ERWDT: Watchdog
- ERDMA: DMA Controller
- ERPLIC: Interrupt Controller
- ERGPIO: GPIO
Need for indigenous Microprocessors - Significant due to the accentuated use of electronic systems and its applications.

Microprocessor Development Programme (MDP) – funded by MeitY, aims to achieve self-reliance in Microprocessor Technology.

C-DAC - responsible for the design and development of a family of Microprocessors, IPs, SoCs and Ecosystem
Objectives

- Development of a series of Processors and reusable peripheral IP cores
- Design and develop a SoC ASIC integrating the 64-bit Quad Core 2GHz RISC Processor with peripheral IPs
- Making available the full Ecosystem for the processor
- Resource Centre - Processors, IPs and eco-system for hardware designers/users of the Microprocessor.
Developed VEGA series of microprocessors including India's first 64-bit multi-core RISC-V based Superscalar Out-of-order Processor.

VEGA series - 32/64-bit Single/Dual/Quad Core Superscalar In-Order /Out-of-Order processor cores based on RISC-V ISA with Multilevel Caches, Memory Management Unit and Coherent Interconnect.

Completed two tape outs and more scheduled in next two years
VEGA Processors

- 32 bit Microcontroller Class
- 64 bit Application Core
- 64 bit, 16 stage High Performance Application Core
- 64 bit, 16 stage High Performance Application Dual Core
- 64 bit, 16 stage High Performance Application Quad Core
Development and fabrication of SoCs integrating VEGA Processors with various System, Communication and Peripheral IPs.

The first VEGA microprocessor-based SoC chip 'THEJAS32', a 32-bit Single core SoC taped out in SilTerra 130nm process.

'THEJAS64', a 64-bit Single core SoC chip taped out in SCL 180nm process.

Design implementation of ‘DHRUV64’, a 64-bit Dual core SoC is in progress. This will be followed by ‘DHANUSH64’, high performance 64-bit Quad core SoC variants.
THEJAS32 SoC ASIC

Key features

- VEGA ET1031 Processor
- 256KB internal SRAM
- UARTs
- SPIs
- TIMERs
- PWMs
- I2C interfaces
- GPIOs
- 3.3V IO
- Frequency: 100MHz
THEJAS64 SoC ASIC

Key features
- VEGA AS1061 Processor
- 128KB internal SRAM
- 256MB SDRAM support
- 64MB Boot Flash via QSPI
- UARTs
- SPI
- TIMERs
- I2C
- GPIOs
- 3.3V IO
- Frequency : 80MHz
ARIES Development Boards

Key features

• Processor : VEGA ET1031
• RAM : 256KB
• Flash : 2MB
• UART : 3 nos
• SPI : 3 nos
• Timer : 3 nos
• PWM : 8 nos
• I2C : 2 nos
• ADC : 4 channel
• GPIO : 32 nos
DHRUV64
SoC

64 bit Dual Core SoC

- Superscalar Out-Of-Order
- Application Core
- 1 GHz CPU Performance
DHANUSH64 SoC

- 64 bit Quad Core SoC
- Superscalar Out-Of-Order
- Multimedia Core
- 2 GHz CPU Performance
VEGA Ecosystem

• Eclipse based IDE
• Operating systems (Linux, Zephyr, FreeRTOS, Fedora, Debian)
• Linux Devices Drivers
• Board support packages
• 75+ libraries for IoT applications
• Compiler Tools
• Documentation
• Discussion forum
• Tutorial videos
Target applications

• Internet-of-Things
• Consumer electronics
• Medical devices
• Power electronics
• Single board computers
• Industrial automation
• Intelligent transportation
Key Benefits

• Strategic advantage - India will own the IP for high-end microprocessors

• Mission Mode project dedicated for total implementation by interaction with academic & industry
Key Benefits

• Silicon based deliverables, directly deployable in products
• Comprehensive hardware and software ecosystem for microprocessor based product design
Key Benefits

• Self-reliance, with clear financial and strategic advantages

• Pave the way to Indian-designed and manufactured electronics chips and hardware - leading to success in MAKE IN INDIA initiative
C-DAC has had the opportunity to be part of the Challenge, launched by MeitY to proliferate use of indigenous microprocessors.

Two SoCs, THEJAS32 and THEJAS64 based on VEGA 32-bit and 64-bit processors made available for the Challenge

The VEGA based SoCs successfully deployed in various designs by the participating teams comprising of academia and start-ups

Actively involved in providing support for the conduct of the challenge.
Swadeshi Microprocessor Challenge
Opportunity

CUSTOM SOC DEVELOPMENT AND DEPLOYMENT
CO-DEVELOPMENT OF ELECTRONIC PRODUCTS BASED ON VEGA PROCESSOR SOC
AFFORDABLE SILICON PROVEN IPS
FASTER PRODUCT TO MARKET THROUGH DEDICATED SUPPORT AND COMPREHENSIVE ECOSYSTEM
VEGA based SoCs