





CDAC – R&D organisation under MeitY

High Performance Computing

Health Informatics

VLSI & Embedded Systems

Professional Electronics

Cyber Security

Software Technologies





Hardware Design Group – Thrust Areas

Product designs for Industrial, Consumer, Automotive and Bio-Medical Applications

Total product implementations using ASIC Technology

IP development for ASIC implementations

ASIC Consultancy Services

Design Verification Services





Expertise

Microprocessor Design

ASIC design and FPGA implementations

Analog and Mixed Signal IC design

High speed PCB design

Embedded System development

Ergonomics, tooling and mechanical design

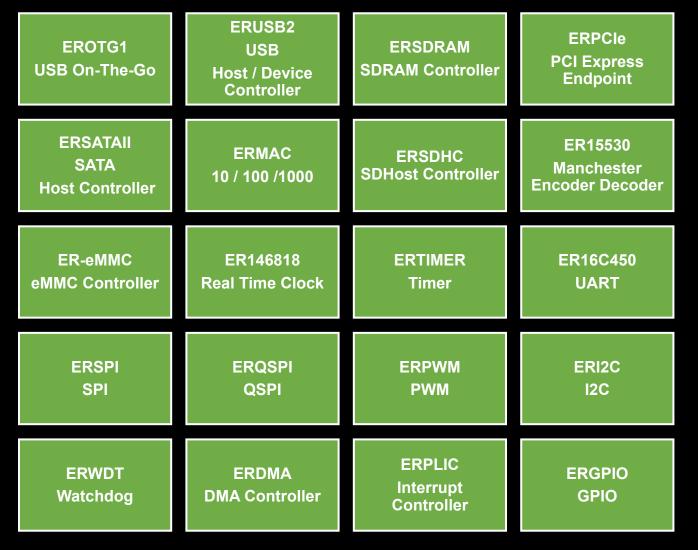
Precision assembly and testing

Field deployment of products and ToT





ASTRA – IP Portfolio







Background

Need for indigenous Microprocessors -Significant due to the accentuated use of electronic systems and its applications.

Microprocessor Development Programme (MDP) – funded by MeitY, aims to achieve self-reliance in Microprocessor Technology.

C-DAC -responsible for the design and development of a family of Microprocessors, IPs, SoCs and Ecosystem





Objectives

Development of a series of Processors and reusable peripheral IP cores

Design and develop a SoC ASIC integrating the 64-bit Quad Core 2GHz RISC Processor with peripheral IPs

Making available the full Ecosystem for the processor

Resource Centre - Processors, IPs and eco-system for hardware designers/users of the Microprocessor.





Status

Developed **VEGA** series of microprocessors including India's first 64-bit multi-core RISC-V based Superscalar Out-of-order Processor.

VEGA series - 32/64-bit Single/Dual/Quad Core Superscalar In-Order /Out-of-Order processor cores based on RISC-V ISA with Multilevel Caches, Memory Management Unit and Coherent Interconnect.

Completed two tape outs and more scheduled in next two years

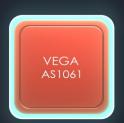




32 bit Microcontroller Class







64 bit Application Core



64 bit, 16 stage High Performance Application Core



64 bit, 16 stage High Performance Application Dual Core



64 bit, 16 stage High Performance Application Quad Core





VEGA SoCs

Development and fabrication of SoCs integrating VEGA Processors with various System, Communication and Peripheral IPs.

The first VEGA microprocessor-based SoC chip 'THEJAS32', a 32-bit Single core SoC taped out in SilTerra 130nm process

'THEJAS64', a 64-bit Single core SoC chip taped out in SCL 180nm process.

Design implementation of '**DHRUV64**', a 64-bit Dual core SoC is in progress. This will be followed by '**DHANUSH64**', high performance 64-bit Quad core SoC variants.

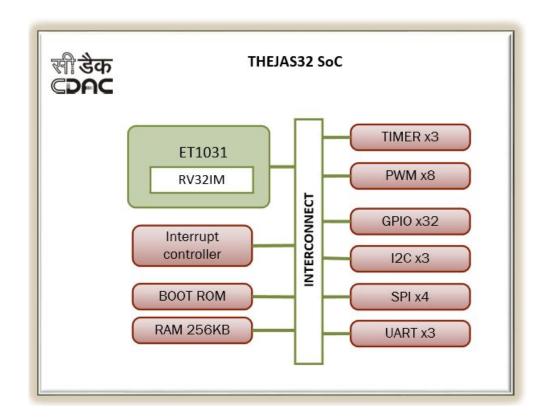


THEJAS32 SoC ASIC

Key features

- VEGA ET1031 Processor
- 256KB internal SRAM
- UARTs
- SPIs
- TIMERs
- PWMs
- I2C interfaces
- GPIOs
- 3.3V IO
- Frequency: 100MHz





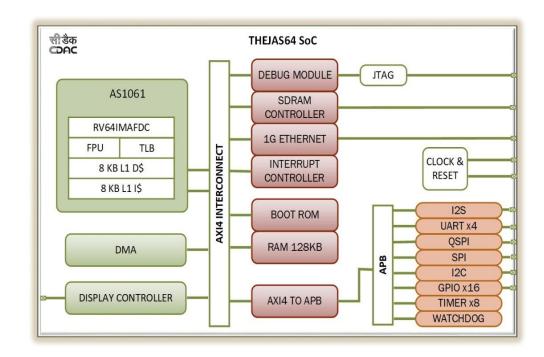


THEJAS64 SoC ASIC

Key features

- VEGA AS1061 Processor
- 128KB internal SRAM
- 256MB SDRAM support
- 64MB Boot Flash via QSPI
- UARTs
- SPI
- TIMERs
- 12C
- GPIOs
- 3.3V IO
- Frequency: 80MHz







ARIES Development Boards

Key features

• Processor : VEGA ET1031

• RAM : 256KB

• Flash : 2MB

• UART : 3 nos

• SPI : 3 nos

• Timer : 3 nos

• PWM:8 nos

• I2C : 2 nos

• ADC : 4 channel

• GPIO : 32 nos





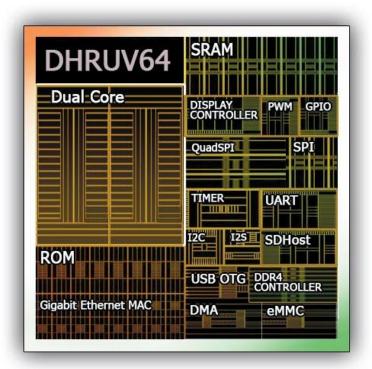




DHRUV64 SoC

64 bit Dual Core SoC

- > Superscalar Out-Of-Order
- > Application Core
- 1 GHz CPU Performance







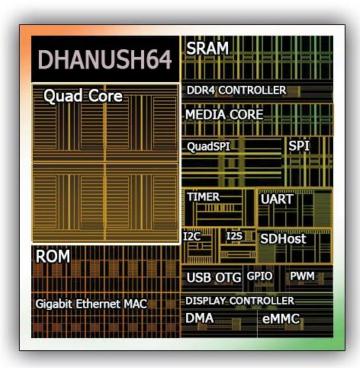
DHANUSH64 SoC

64 bit Quad Core SoC

> Superscalar Out-Of-Order

Multimedia Core

> 2 GHz CPU Performance



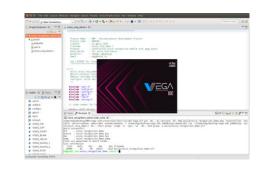




- Eclipse based IDE
- Operating systems (Linux, Zephyr, FreeRTOS, Fedora, Debian)
- Linux Devices Drivers
- Board support packages
- 75+ libraries for IoT applications
- Compiler Tools
- Documentation
- Discussion forum
- Tutorial videos













Target applications

- Internet-of-Things
- Consumer electronics
- Medical devices
- Power electronics
- Single board computers
- Industrial automation
- Intelligent transportation



Key Benefits

•Strategic advantage - India will own the IP for high-end microprocessors

 Mission Mode project dedicated for total implementation by interaction with academic & industry



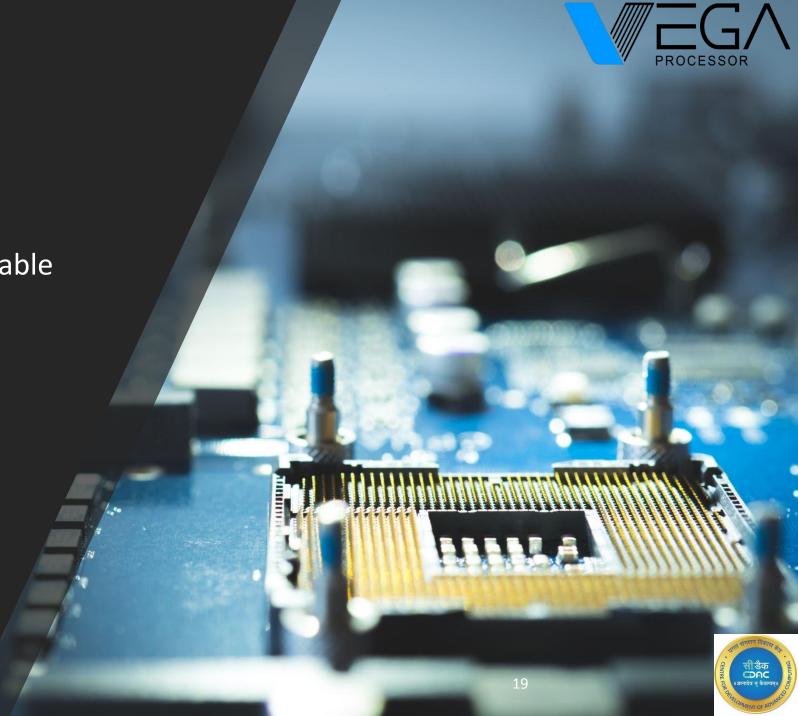
Industry

Private Organizations

Key Benefits

 Silicon based deliverables, directly deployable in products

 Comprehensive hardware and software ecosystem for microprocessor based product design







Key Benefits

•Self-reliance, with clear financial and strategic advantages

 Pave the way to Indian-designed and manufactured electronics chips and hardware - leading to success in

MAKE IN INDIA initiative





आत्मनिर्भर भारत.

AATMANIRBHAR BHARAT.



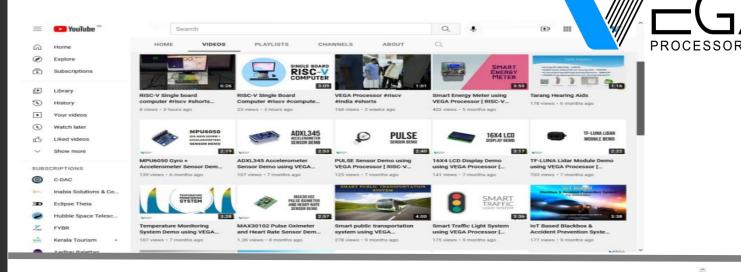


Swadeshi Microprocessor Challenge

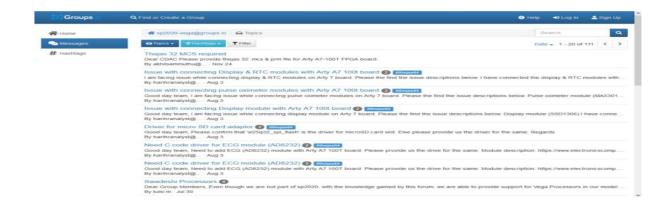
- C-DAC has had the opportunity to be part of the Challenge, launched by MeitY to proliferate use of indigenous microprocessors.
- Two SoCs, THEJAS32 and THEJAS64 based on VEGA 32-bit and 64-bit processors made available for the Challenge
- The VEGA based SoCs successfully deployed in various designs by the participating teams comprising of academia and start-ups
- Actively involved in providing support for the conduct of the challenge.



Swadeshi Microprocessor Challenge









Opportunity





CUSTOM SOC DEVELOPMENT AND DEPLOYMENT



CO-DEVELOPMENT OF ELECTRONIC PRODUCTS BASED ON VEGA PROCESSOR SOC



AFFORDABLE SILICON PROVEN IPS



FASTER PRODUCT TO MARKET THROUGH DEDICATED SUPPORT AND COMPREHENSIVE ECOSYSTEM





THANK YOU



VEGA based SoCs

